ABSTRACT OF THE DISCLOSURE

A demultiplexer is provided capable of handing different types of the multiplexing format and minimizing the overall size and the cost of its circuitry arrangement.

A controller 113 is arranged responsive to the micro-code read out in a sequence from a command memory 111 for generating control signals for controlling the components. Received packets of data are saved in a shift register 102 and their headers are registered in a group of registers 103 when desired before analyzed in a calculating unit 104. The destination of the packets is determined from the packet ID in the header by an output destination determining unit 105. A separator 106 upon examining an output of the calculating unit 104 and a result of the destination determination, separates desired packets from the data output of the shift register 102 and transfers them to the destination determined. Also, a timing data is extracted from the received packet data and transferred to a clock controller 114 for controlling the system clock. As the different types of the multiplexing format are handled by modifying the micro-codes read out from the command memory 111, the overall size and the cost of the circuitry arrangement will successfully be reduced.